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09/870,446	06/01/2001	Michael Catherwood	18153.0046	8454

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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/870,446	Applicant(s) CATHERWOOD, MICHAEL	
	Examiner Shane F Gerstl	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/16/01, 9/28/01, and 6/01/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-13 have been examined.

Papers Received

2. Receipt is acknowledged of drawings and information disclosure statement papers submitted, where the papers have been placed of record in the file.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 303. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Trapping Based on Trap Flags Corresponding to Pointer Registers On a System Power-up or Reset.

Oath/Declaration

5. Applicant has not given a post office address anywhere in the application papers as required by 37 CFR 1.33(a), which was in effect at the time of filing of the oath or declaration. A statement over applicant's signature providing a complete post office address is required.

Information Disclosure Statement

6. The information disclosure statement filed 16 November 2001 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. There are multiple recitations and copies of the following US patents in the information disclosure statement: 6,145,049; 5,327,566; 5,642,516; and 6,128,728. The references cited in the information disclosure statement have been considered.

Claim Objections

7. Claim 7 is objected to because of the following informalities: the claim states the phrase, "a pointer register with a trap flag set to reset," which is somewhat unclear. Examiner suggests that the phrase read, "a pointer register corresponding to a trap flag set to a reset condition," so that consistent claim language is used within the set of claims regarding to the relationship between the pointer registers and trap flags and with respect to the clarifying that the trap flag is set to a reset condition as done in the other sets of claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-4, 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Cotton (3,771,146).

10. In regard to claim 1, Cotton discloses a method of preventing processing errors due to invalid pointers, comprising:

a. fetching an instruction having a pointer operand for execution; Column 8, lines 17-18 show that instructions are fetched. Column 5, lines 17-22 show that performance of each process (instruction or set of instructions) uses a capability register for a required access to memory (and thus holds an operand since the value is necessary for operation). Lines 24-44 show that the registers hole data that is based on a pointer table and thus the capability registers hold pointer operands.

b. determining whether a trap flag corresponding to the pointer is in a set or reset condition; Column 5, lines 24-27 and 45-48 show that the pointer register includes an access field (trap flag) for holding access code that is used for trapping a process. Column 17, lines 34-42 show a case where a trap is caused when the access code (trap flag) is '00' or reset, and thus the fact that the flag is in a reset condition was determined.

c. and generating a trap control signal when the trap flag is in a reset condition. Column 17, lines 34-42 show a case where a trap is caused when the access code (trap flag) is '00' or reset. Column 11, lines 32-36 shows that the setting of the trap indicator causes a trap signal to be passed (and thus generated) to a control unit and it is thus a trap control signal.

11. In regard to claim 2, Cotton discloses the method according to claim 1, further comprising: triggering a trap interrupt based on the trap control signal. Column 11, lines 29-36 show that the trap signal sent to the control unit triggers a trap micro-sequence to be performed. The heading given in column 10, line 16 shows that the trap operation is that of a trap interrupt.

12. In regard to claim 3, Cotton discloses the method according to claim 1, further comprising: executing the instruction. Column 2, lines 63-65 show that the processes (instructions) are executed. Further, column 4, lines 14-16 show an instruction that is executed. There are similar statements throughout the disclosure that indicate that the fetched instructions are in fact executed.

13. In regard to claim 4, Cotton discloses the method according to claim 1, further comprising: changing the trap flag corresponding to the pointer from the reset condition to the set condition based upon a write to the pointer. As shown in the sections cited above for claim 1, the access code (trap flag) indicates the access rights to the pointer section of the capability register. This is further shown in column 1, lines 13-26, which illustrates that the access code is for a certain pertinent capability word (pointer). This means that when the pointer changes, the access code (trap flag) corresponding to the pointer must inherently change as well so that it gives updated access rights to the memory section pointed to.

14. In regard to claim 9, Cotton discloses a processor that prevents processing errors due to invalid pointers, comprising:

a. instruction fetch and decode logic for fetching and decoding instructions; Column 8, lines 17-18 show that instructions are fetched and thus there is instruction fetch logic. The decoding logic is inherent since the processor executes instructions or processes, as discussed in both the background and general description sections, and there must be decoding logic to interpret the machine instructions in order to recognize the operation to be performed and the operands to use for the operation.

d. registers; Column 5, lines 17-22 show that performance of each process (instruction or set of instructions) uses a capability register for a required access to memory.

b. trap flags, each corresponding to a register and each indicating a set or reset condition; Column 5, lines 24-27 and 45-48 show that the pointer register includes an access field (trap flag) for holding access code that is used for trapping a process. Column 17, lines 34-42 show a case where a trap is caused when the access code (trap flag) is '00' or reset. Column 10, lines 5-15 show that the access code (trap flags) are manipulated to determine if they are in a set or reset condition (a '1' or '0').

e. and a pointer trap coupled to the trap flags, the pointer trap generating a trap control signal based on decoding an instruction that reads a register that has a corresponding trap flag in a reset condition. Lines 24-44 show that the registers hole data that is based on a pointer table and thus the capability registers hold pointer operands. Column 17, lines 34-42 show a case where a trap is caused

when the access code (trap flag) is '00' or reset. Column 11, lines 32-36 shows that the setting of the trap indicator causes a trap signal to be passed (and thus generated) to a control unit and it is thus a trap control signal.

15. In regard to claim 10, Cotton discloses the processor according to claim 9, wherein the trap control signal is only generated when the register being read from is acting as a pointer register. As shown above, the registers being read from are pointer registers.

16. In regard to claim 11, Cotton discloses the processor according to claim 9, further comprising interrupt logic for generating an interrupt based on the trap control signal. Column 11, lines 29-36 show that the trap signal sent to the control unit triggers a trap micro-sequence to be performed. The heading given in column 10, line 16 shows that the trap operation is that of a trap interrupt.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 5-8 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cotton (3,771,146) in view of Appelt (3,886,524).

19. In regard to claim 5,

a. Cotton discloses the method according to claim 1, comprising changing the trap flag to the reset condition. Column 5, lines 53-58 show that the

capability is register (which includes the trap flag or access code) is reset on various conditions.

b. Cotton does not disclose changing the trap flag to the reset condition after one of a power up of the processor or a reset of the processor.

c. Appelt has disclosed in column 9, lines 30-48 that a TLPRES- signal is set to a reset condition of "low" ('0') after recognizing a rest of the processor will occur. This then causes a power-up interrupt trap to be performed and is thus indicates a trap and is a trap flag.

d. Appelt shows in this same section that this trap flag prohibits activity from occurring on the reset since the results will be unknown and cannot be processed correctly with a reset of power to the processor. The power-up trap is a recovery-type trap that allows for resuming of processing when there is stable power. This ability to prohibit activity when the processor is unstable and thus avoid errors would have motivated one of ordinary skill in the art to modify the design of Cotton to set the trap flag to a reset condition on a processor reset as taught by Appelt.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Cotton to incorporate the method of setting the trap flag to a reset condition on a processor reset as taught by Apelt so that data instability and processing errors are avoided.

20. In regard to claim 6,

a. Cotton discloses a method of preventing processing errors due to invalid pointers, comprising:

i. providing trap flags, each corresponding to a pointer register; Column 5, lines 17-22 show that performance of each process uses a capability register for a required access to memory. Lines 24-44 show that the registers hole data that is based on a pointer table and thus the capability registers hold pointer operands. Column 5, lines 24-27 and 45-48 show that the pointer register includes an access field (trap flags) for holding access code that is used for trapping a process.

ii. resetting the trap flags; Column 5, lines 53-58 show that the capability is register (which includes the trap flags or access code) is reset on various conditions.

iii. and setting the trap flag corresponding to each pointer register based on the pointer register being written. As shown in the sections cited above, the access code (trap flag) indicates the access rights to the pointer section of the capability register. This is further shown in column 1, lines 13-26, which illustrates that the access code is for a certain pertinent capability word (pointer). This means that when the pointer changes, the access code (trap flag) corresponding to the pointer must inherently change as well so that it gives updated access rights to the memory section pointed to.

b. Cotton does not disclose that the resetting of the trap flags is based on a power-up or reset.

c. Appelt has disclosed in column 9, lines 30-48 that a TLPRES- signal is set to a reset condition of "low" ('0') after recognizing a rest of the processor will occur. This then causes a power-up interrupt trap to be performed and is thus indicates a trap and is a trap flag.

d. Appelt shows in this same section that this trap flag prohibits activity from occurring on the reset since the results will be unknown and cannot be processed correctly with a reset of power to the processor. The power-up trap is a recovery-type trap that allows for resuming of processing when there is stable power. This ability to prohibit activity when the processor is unstable and thus avoid errors would have motivated one of ordinary skill in the art to modify the design of Cotton to set the trap flag to a reset condition on a processor reset as taught by Appelt.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Cotton to incorporate the method of setting the trap flag to a reset condition on a processor reset as taught by Apelt so that data instability and processing errors are avoided.

21. In regard to claim 7, Cotton in view of Appelt discloses the method according to claim 6, further comprising: generating a trap control signal when an instruction reads a pointer register with a trap flag set to reset. Column 17, lines 34-42 show a case where a trap is caused when the access code (trap flag) is '00' or reset. Column 11, lines 32-

36 shows that the setting of the trap indicator causes a trap signal to be passed (and thus generated) to a control unit and it is thus a trap control signal.

22. In regard to claim 8, Cotton in view of Appelt discloses the method according to claim 7, further comprising: triggering a trap interrupt based on the trap control signal. Column 11, lines 29-36 show that the trap signal sent to the control unit triggers a trap micro-sequence to be performed. The heading given in column 10, line 16 shows that the trap operation is that of a trap interrupt. Further, Appelt shows in column 9, lines 46-48 that the power-up trap is an interrupt trap.

23. In regard to claim 12,

a. Cotton discloses the processor according to claim 9, further comprising: resetting the trap flags. Column 5, lines 53-58 show that the capability is register (which includes the trap flags or access code) is reset on various conditions.

b. Cotton does not disclose a reset/power up unit coupled to the trap flags, the reset/power on unit resetting the trap flags upon a reset/power up.

c. Appelt has disclosed in column 9, lines 30-48 that a TLPRES- signal is set to a reset condition of "low" ('0') after recognizing a rest of the processor will occur. This then causes a power-up interrupt trap to be performed and is thus indicates a trap and is a trap flag. There inherently exists reset logic or a rest unit in this disclosure to perform this resetting of the trap flags.

d. Appelt shows in this same section that this trap flag prohibits activity from occurring on the reset since the results will be unknown and cannot be processed correctly with a reset of power to the processor. The power-up trap is

a recovery-type trap that allows for resuming of processing when there is stable power. This ability to prohibit activity when the processor is unstable and thus avoid errors would have motivated one of ordinary skill in the art to modify the design of Cotton to set the trap flag to a reset condition on a processor reset using a reset unit as taught by Appelt.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Cotton to incorporate the method of setting the trap flag to a reset condition on a processor reset using a reset unit as taught by Apelt so that data instability and processing errors are avoided.

24. In regard to claim 13,

a. Cotton discloses the processor according to claim 9, further comprising: a trap flag control unit coupled to the trap flags, the trap flag control unit resetting the trap flags and setting each trap flag based on the corresponding register having been written by an instruction. Column 5, lines 53-58 show that the capability is register (which includes the trap flags or access code) is reset on various conditions. As shown in the sections cited above for claim 1, the access code (trap flag) indicates the access rights to the pointer section of the capability register. This is further shown in column 1, lines 13-26, which illustrates that the access code is for a certain pertinent capability word (pointer). This means that when the pointer changes, the access code (trap flag) corresponding to the pointer must inherently change as well so that it gives updated access rights to

the memory section pointed to. This is all inherently accomplished using logic for setting the trap flags or a trap flag control unit.

b. Cotton does not disclose resetting the trap flags upon a reset/power up.

c. Appelt has disclosed in column 9, lines 30-48 that a TLPRES- signal is set to a reset condition of "low" ('0') after recognizing a rest of the processor will occur. This then causes a power-up interrupt trap to be performed and is thus indicates a trap and is a trap flag. There inherently exists reset logic or a rest unit in this disclosure to perform this resetting of the trap flags.

d. Appelt shows in this same section that this trap flag prohibits activity from occurring on the reset since the results will be unknown and cannot be processed correctly with a reset of power to the processor. The power-up trap is a recovery-type trap that allows for resuming of processing when there is stable power. This ability to prohibit activity when the processor is unstable and thus avoid errors would have motivated one of ordinary skill in the art to modify the design of Cotton to set the trap flag to a reset condition on a processor reset using a reset unit as taught by Appelt.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Cotton to incorporate the method of setting the trap flag to a reset condition on a processor reset using a reset unit as taught by Apelt so that data instability and processing errors are avoided.

Conclusion

25. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

26. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents have been cited to further show the art with respect to trapping and resetting in general.

US Pat No 6,412,081 to Koscal shows a power-on-reset process that enables a trap.

US Pat No 4,779,191 to Greenblatt discloses the use of a trap if an attempt is made to use an invalid pointer.

US Pat No 4,408,273 to Wheatley teaches trapping based on a register contents, which holds a pointer.

US Pat No 4,074,353 to Woods shows how to trap when there is an invalid memory access.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
April 16, 2004

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